Code No.: 9A04605/R09

B.Tech. III Year II Semester Regular & Supplementary Examinations

Set-3

April/May - 2013

VLSI DESIGN

(Common to ECE, EIE and E.Con.E)

Time: 3 Hours | Max. Marks: 70

*Answer any **FIVE** Questions*

***All** Questions carry **equal** marks*

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1. (a) Write important characteristics of CMOS.
   (b) Why CMOS is preferred over bipolar technology?
   (c) Short notes on advanced CMOS fabrication technologies.

2. Mention different non-ideal I-V effects and clearly explain about them.

3. (a) What are the effects of scaling on V_t?
   (b) Discuss the limits due to sub threshold currents.

4. What is the problem of driving large capacitance load? Explain a method to drive such load.

5. Implement a 4-bit ALU using adder as basic primitive block and explain how the arithmetic and logical operations are performed using adder element.

6. (a) Differentiate between chips with programmable logic structure and chips with programmable interconnect. Give an example for each.
   (b) Give a brief description of various methods of programming the Programmable Array Logic (PALs) in CMOS.

7. (a) What is Register Transfer Level (RTL) synthesis?
   (b) Explain with an example how RTL description in VHDL capture the attributes of a design.

8. (a) Write about different fault models.
   (b) List out all the possible struck at faults for three input NAND gate and thus generate the minimum test vectors that detect all the faults.